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Multiobjective design optimization of transformers for battery cell balancing converters considering bidirectional power flow

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Abstract

Owing to an increase in the demand for bidirectional applications such as battery energy storage systems (BESS), isolated bidirectional converters have become more popular. However, conventional transformer design methods such as the area product and core geometrical coefficient methods, consider only one operating point. Thus, these do not always guarantee high efficiency if there are any changes in the operation point of the converter. Accordingly, this paper proposes a multiobjective optimized transformer design algorithm that considers the overall energy loss of the bidirectional operation of the converter. The proposed algorithm adopts a nondominated sorting genetic algorithm-II (NSGA-II) effective core cross-sectional area and turn ratios as main variables. A 20W prototype converter with a transformer for 20-series lithium-ion cell balancing purposes has been built for verification. The results show that the proposed algorithm dissipates lower power loss during the charge and discharge mode of operations with a smaller volume than the conventional method.

Keywords Battery applications · Bidirectional converter · Multiobjective optimization · Transformer design

1 Introduction

Because renewable energy, battery energy storage systems (BESS), electric vehicles, and smart grids are being widely used, the battery market is growing, and accordingly, the demand for battery chargers is also increasing [1, 2]. A typical battery charger consists of a unidirectional topology that transfers power from an input power source to a battery. However, to be applied to a BESS, a battery charger must be configured with a bidirectional converter [3]. Furthermore, if isolation is essential for safety reasons, battery chargers should be isolated by a high-frequency transformer [4].

For transformer design, simple and practical methods such as the area product (A_p) method and the core geometrical coefficient (K_{gfe}) method are commonly used [5–7]. The area product is a parameter that represents the product of the

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¹ Department of Electrical, Electronic and Computer Engineering, University of Ulsan, Ulsan, Republic of Korea effective core cross-sectional area (A_e) and the window area (A_{cw}) , and is directly related to the power handling capability of the transformer. It provides a measure of core utilization and determines the maximum amount of power that a transformer can handle without saturation. A higher A_p value indicates a larger core cross-sectional area or a larger window area, which allows for a higher magnetic flux density or magnetic field intensity. This in turn, makes it possible to achieve a higher power handling capacity. In addition, K_{gfe} represents the effective size of the core in terms of the combined impact of the copper loss and the core loss. Considering these losses, it provides a more accurate estimation of the power handling capability and overall efficiency of the transformer.

However, conventional transformer design methods consider only one operating point. In unidirectional battery charging applications, even in the constant current and constant voltage (CC–CV) charging processes, efficiency should be considered for various output current conditions [8, 9]. To complete the changed sequence, the duty is changing during operation, which results in different RMS currents in the transformer. Furthermore, for bidirectional converters, high efficiency should be ensured in both the charging and discharging modes under wide duty variations [10–12].



To address this challenge, this paper proposes a multiobjective design optimization algorithm for transformers in bidirectional converters. The proposed algorithm optimizes the core volume, the transformer loss, and the operating duty with the transformer design parameters. For optimized design candidates, PLECS simulation is utilized to analyze total converter efficiency to choose a final solution.

The remainder of this paper is organized as follows. Bidirectional converter applications and conventional transformer design methods are reviewed in Sect. 2. The proposed design algorithm and simulation results are shown in Sect. 3. Verification through hardware experiments is shown in Sect. 4. Finally, some concluding remarks are made in Sect. 5.

2 Target application and conventional transformer design methods

2.1 Bidirectional converter operation in cell balancing applications

Figure 1 shows the target system configuration. In this active cell balancing system, the battery pack consists of 20 cells and the bidirectional converter equalizes the cell voltages by redistributing the charge from the pack to the cell (buck mode)





Fig. 1 Bidirectional battery cell balancing converter: **a** whole converter configuration; **b** bidirectional forward converter

or from the cell to the pack (boost mode). The bidirectional converter is configured as the two-switched forward topology shown in Fig. 1a and waveforms for its bidirectional operation are shown in Fig. 2. The specifications of the converter are shown in Table 1. Bidirectional operation of the converter is controlled by duty signal alternation. When the converter is controlled by the on-duty of Q_1 and Q_2 , D_{buck} , current flows from the battery pack to the cell. Thus, the converter operates in the buck mode. When the converter is controlled by the on-duty of D_{boost} , the current flows from the cell to the battery pack [13, 14]. Thus, the converter operates in the boost mode. $D_{boundary}$ is the duty that makes the current go to zero. Thus, it is referred to as the boundary duty. D_{buck} , D_{boost} , and $D_{boundary}$ are related to the circuit parameters as follows:

$$D = \begin{cases} \frac{(V_{cell} + I_L(r_{bal} + r_L)) \cdot N}{V_{pack}} (Buck \ mode) \\ \frac{(V_{cell} - I_L(r_{bal} + r_L)) \cdot N}{V_{pack}} (Boost \ mode) \end{cases}$$
(1)

$$D_{boundary} = \frac{(V_{cell})N}{V_{pack}}$$
(2)

where V_{cell} is the open-circuit voltage of the cell, I_L is the average inductor current, r_L is the equivalent series resistance



Fig. 2 Proposed converter operation waveforms: a buck mode; b boost mode

 Table 1
 Bidirectional converter specifications

| Name | Symbol | Value |
|----------------------------|------------|---------------|
| Voltage of the pack | V_{pack} | 76 V |
| Voltage of cells | V_{cell} | 4~3.6 V |
| Switching frequency | f_{sw} | 50 kHz |
| Output inductor | L | $500 \ \mu H$ |
| Primary filter capacitor | C_1 | 55 µF |
| Secondary filter capacitor | C_2 | $200 \ \mu F$ |



Fig. 3 Inductor current change according to the operation duty

of the output inductor, r_{bat} is the equivalent series resistance of the cell, N is the turn ratio of the transformer, and V_{pack} is the open circuit voltage of 20 series-connected cells. The operation duty is greatly affected by the transformer turn ratio. From (3), the inductor current change according to the operation duty is shown in Fig. 3.

$$I_{L} = \begin{cases} \frac{D\frac{V_{pack}}{N} - V_{cell}}{(r_{bal} + r_{L})} (Buck \ mode) \\ \frac{V_{cell} - D\frac{V_{pack}}{N}}{(r_{bal} + r_{L})} (Boost \ mode) \end{cases}$$
(3)

Since the average inductor current is decided by the duty, the RMS inductor current for each of the transformer designs is different, which has a great influence on the converter efficiency (Fig. 4).

The switch matrix selects the target cell to be charged or discharged. In the buck mode, the single cell with the lowest voltage among the cells is connected to the secondary. On the other hand, the cell with the highest voltage is connected to the secondary in the boost mode for discharging. Likewise, 20 cells are connected one by one to equalize the charge inside the pack.

2.2 Conventional transformer design method and its limitations

Typically, the most straightforward and practical method for transformer design is the area product method. This method utilizes a fundamental concept: the size of the magnetic core is determined by the power handling and allowed core losses of the transformer. The method based on the geometric constant (K_{gfe}) of the magnetic core is an extension of the area product method that includes the optimization of





Fig. 4 Flow chart of the proposed algorithm

the transformer loss. It aims to achieve optimal transformer design by searching for the condition that minimizes both the total losses and the size of the core [7, 15]. The core selection criterion of the area product method is expressed as (4) and the core selection criteria of the K_{gfe} method are expressed as (5) and (6).

$$A_e A_{cw} \ge A_p = \frac{P_{tot} \bullet 10^4}{B_{ac} f_{sw} J K_f K_u},\tag{4}$$

$$K_{gfe} = \frac{A_{cw}(A_e)^{(2(\beta-1)/\beta)}}{MLTl_m^{(2/\beta)}} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)} \right]^{-\left(\frac{\beta+2}{\beta}\right)}$$
(5)

$$K_{gfe} \ge K_{gfe,ref} = \frac{\rho \lambda_1^{2} I_{tot}^{2} K_{fe}^{(\frac{2}{\beta})}}{4K_u(P_{tot})^{((\beta+2)/\beta)}}$$
(6)

where A_e and A_{cw} are the effective cross-sectional area and the window area of the core, P_{tot} is the total power of the transformer, B_{ac} is the operating flux density of the core, f_{sw} is the switching frequency, J is the current density, K_f and K_u are the waveform factor and the window utilizing factor, *MLT* is the mean length per turn of the core, l_m is the effective length of the magnetic path, β is the flux density exponent, ρ is the resistivity of copper, λ_1 is the applied primary volt-seconds, and the I_{tot} is total current of the transformer.

Although the area product and K_{gfe} methods are simple and practical, they have several disadvantages. First, several iterations of trial and error in the design process may be required to satisfy conditions (4) and (6) [16]. Second, duty changes according to the bidirectional operation of the converter are not considered. Conventional transformer design methods only determine the core size for one operating condition. Therefore, it is not possible to consider a power loss that varies due to a change in the operating current or a change in duty during bidirectional operation. Therefore, conventional transformer design methods do not always guarantee high energy efficiency that considers the overall operation. To mitigate these issues, the transformer design should be optimized for both buck and boost modes while considering the actual operation duty excursions.

3 Proposed algorithm

3.1 Multiobjective optimization

In the proposed transformer design algorithm, a multiobjective optimization algorithm called nondominated sorting algorithm-II (NSGA-II) is adopted. NSGA-II has two outstanding advantages. It increases the possibility of survival of the wellevaluated variables in the fitness function by nondominated sorting, and it provides a constant distance between optimized solutions to obtain multiple design solutions by crowding distance sorting [17].

In the proposed method, the performance vector (7) is minimized over the parameter vector \vec{x} defined in (8)

$$\operatorname{Min}_{\vec{x}} J = \left[V_{core}, P_{transformer}, \left| D_{boundary, ref} - D_{boundary} \right| \right], \quad (7)$$

$$\vec{x} = \left(N, A_e, N_p\right)^T \tag{8}$$

where N is the transformer turn ratio, A_e is the effective core cross-sectional area, N_p is the primary winding number, and V_{core} is the core volume which is calculated from A_e according to the core datasheet. $P_{transformer}$ is the total transformer power loss.

In calculating $P_{transformer}$, the core volume P_{core} and the copper loss P_{copper} are considered together, and expressed by:

$$P_{transformer} = P_{core} + P_{copper} \tag{9}$$

$$P_{core} = \frac{8}{\pi^2 [4D(1-D)]^{\gamma+1}} k_{fe} f_{sw}^{\ \alpha} B_{ac}^{\ \beta} V_{core}, \tag{10}$$

$$P_{copper} = \frac{\rho N_x MLT}{W_a} I_{rms}^2 \tag{11}$$

where (10) is from the rectangular extended Steinmetz equation [18] and D is either D_{buck} or D_{boost} depending on the operating mode.

 $D_{boundary}$ is also optimized to ensure the various conversion gains in both the buck and boost modes. To cope with the changing load conditions of the converter in the closed loop, both modes must have an appropriate operating duty range. Since $D_{boundary}$ is responsible for the boundary operating point between two modes, $D_{boudnary,ref}$ must be chosen to fit the specifications of applications where $D_{boundary,ref}$ is the targeted boundary duty value. In this paper, $D_{boundary,ref}$ is chosen to be 0.25 since the duty of the forward converter is limited from 0 to 0.5 to ensure core rest time.

A flow chart of the proposed algorithm is shown in Fig. 5. The algorithm proceeds by a number of steps.

- 1. Choose initial values for the parameters N, A_e , and N_p .
- 2. Calculate the core volume and winding configurations from the chosen parameters.
- 3. Calculate the total transformer power loss and $D_{boundary}$.
- 4. Plot V_{core} , $P_{transformer}$, and $D_{boundary}$ in the Pareto front for the optimized solutions. If the generation reaches the maximum generation limit, stop NSGA-II, plot the Pareto front, and proceed to step 5. Otherwise, repeat steps $1 \sim 4$.
- For the solution candidates in the optimized Pareto front, PLECS simulation is accompanied by MATLAB Simulink to analyze the overall power and energy efficiency at every duty point of the converter for the buck and the boost modes.
- 6. Finally, choose the final solution from the simulation result.



Fig. 5 Winding configuration of an EE core transformer

3.2 Transformer magnetic modeling

In this paper, the EE core shape is chosen for the design due to its popularity. However, the proposed algorithm can be adapted to any core shape without loss of generality. The half-side configuration of the EE core transformer is shown in Fig. 5. The transformer winding is wound in a sandwich configuration to reduce the leakage inductance. Permeance-based equivalent circuit models for the core are shown in Fig. 6. In Fig. 6a, the permeances are placed along the effective magnetic paths of the core and P_{air} are placed for the leakage path through the air [19, 20]. In addition, G_m is the magnetic conductance to model the core loss. The core loss is expressed as:

$$P_{core} = F\dot{\Phi} = \dot{\Phi}^2 G_m \tag{12}$$

$$R_m = \frac{\left(\frac{V_p}{N_p}\right)^2}{P_{core}} \tag{13}$$

$$R_{p,winding} = \frac{\rho N_p MLT}{W_a} \tag{14}$$

$$R_{s,winding} = \frac{\rho N_s M L T}{W_a} \tag{15}$$

where P_{core} is the core loss of the transformer from Eq. (10), F is the magnetomotive force, and Φ is the flux along the core. R_m is the core loss resistance, which is reflected to the electric port, and $R_{p,winding}$ and $R_{s,winding}$ are the winding resistances for the primary and secondary windings.

Considering the geometric symmetry of the core, the magnetic model is simplified to Fig. 6b, and it is implemented by the PLECS magnetic library. The power efficiency and energy efficiency simulation circuits with transformer magnetic modeling are shown in Figs. 7 and 8, respectively.

3.3 NSGA-II optimization results

The NSGA-II design algorithm generates 200 design samples for each generation until it reaches the maximum number of generations. The algorithm setting and generated Pareto front are shown in Table 2 and Fig. 9. After the algorithm generates 200 design candidates, it forwards the corresponding parameter vectors to the PLECS co-simulation part.





Fig. 6 Magnetic circuit model of the transformer in Fig. 5: a permeance circuit model; b simplified model

3.4 PLECS simulation results

From the 200 design candidates, PLECS executes a power and energy efficiency simulation to choose the most optimized design solution. The converter power efficiency simulation result is then sorted in descending order as shown in Fig. 10. Among the ranked design samples three candidates are chosen by the following criterion.



Fig. 7 PLECS power efficiency simulation schematic





Fig. 8 PLECS energy efficiency simulation schematic: a converter circuit with a battery subsystem; b battery subsystem

Table 2 NSGA-II algorithm setting

| Name | Value |
|-------------------------------|-------|
| Population size | 200 |
| Probability of crossover | 0.9 |
| Probability of mutation | 0.5 |
| Maximum number of generations | 50 |
| Mutation strength | 0.05 |
| | |



Fig. 9 Computed Pareto front



Fig. 10 200 design candidates from the last Pareto front

Table 3 Design parameters of the K_{gfe} method

| Name | Symbol | Value |
|--------------------------------|-------------------|---------------------------|
| Turn ratio | Ν | 5 |
| Number of windings | N_p : N_s | 40:8 |
| Effective cross-sectional area | A_e | $52.5 \ mm^2$ |
| Window size area | A_{cw} | 87 <i>mm</i> ² |
| Core volume | V _{core} | 3020 mm ³ |

 Table 4
 Energy efficiency simulation test results

| Name | Symbol | Candidate #1 | Candidate #2 | Candidate #3 |
|------------------------|-------------------|----------------------|----------------------|----------------------|
| Turn ratio | N | 5.96 | 5.07 | 4.9 |
| Number of windings | N_p : N_s | 30.8:5.17 | 36.7:7.24 | 42.0:8.58 |
| Core volume | V _{core} | 3006 mm ³ | 1969 mm ³ | 1476 mm ³ |
| Energy effi- ciency | η_{energy} | 85.83% | 86.12% | 86.33% |



Fig. 11 Designed test samples

- Candidate #1 has the same volume as the conventional transformer design by the K_{gfe} method, which is shown in Table 3, and a higher efficiency among the candidates with same volume.
- Candidate #2 has an intermediate volume between candidates #1 and #3 with the highest efficiency among the same volume.
- Candidate #3 has the smallest volume available on the market and the highest efficiency among candidates with the same volume.

The design parameters for the three candidates and energy efficiency simulation results are summarized in Table 4. With the three design candidates, the converter energy efficiency simulation was carried out. This simulation proceeded until all of the cells were balanced from the same cell



Fig. 12 Test equipment setup

 Table 5
 Parameters for the experimental setup

| Name | Value |
|--------------------------------|---------------|
| Pack voltage V _{pack} | 76 V |
| V _{cell} (buck mode) | 3.6 V |
| V_{cell} (boost mode) | 4 V |
| Load resistance (buck mode) | 1.8 Ω |
| Load resistance (boost mode) | $1.2 k\Omega$ |

condition. For the simulation result, solution #3 is chosen for the hardware test sample parameter.

4 Hardware verification

4.1 Experimental setup

Two transformer samples are made according to Table 4. The nearest core volume in the market is chosen for hardware verification. Transformer test samples and their parameters are shown in Fig. 11 and Table 6. To validate the effectiveness of the proposed algorithm, a 20W prototype converter for 20-series lithium-ion cell balancing is built and tested. For the hardware verification, three experiments were established. First, a power efficiency comparison test with various load conditions between the proposed and conventional designs was performed. Next, a power efficiency time trend test was used to check the energy efficiency of the converter during mode changes.

The equipment setup is shown in Fig. 12, and the parameters are shown in Table 5. For the power efficiency test scenario, the converter operates in the CC mode with various reference current values from 0.5A to 3.0A to check the converter efficiency for the various operation duty values. For the buck mode test, the battery pack is emulated by a





Fig. 13 Converter efficiency test results in different CC conditions: a buck mode; b boost mode

battery emulator (KERNEL BTU-1601-DH), and the electric load in the CV mode is connected to the secondary side to emulate the cell, $V_{cell,buck}$. For the boost mode test, the battery emulator with $V_{cell,Boost}$ is connected to the secondary side, and the electric load in the CV mode is connected Table 6 Hardware design parameters of the test samples

| Parameter | K _{gfe} | Proposed |
|----------------------------------|---------------------------|----------------------|
| Core material | TDK ferrite N87 | |
| Core part number | EE25/13/7 | EE20/10/6 |
| Effective cross-sectional area | $52.5 mm^2$ | $32.1 \ mm^2$ |
| Window size area | 87 <i>mm</i> ² | $57.4 \ mm^2$ |
| Core volume | 3020 mm ³ | 1490 mm ³ |
| Number of windings N_p : N_s | 40:8 | 44:9 |
| Primary winding area | $0.3 \ mm^2$ | $0.16 \ mm^2$ |
| Secondary winding area | $0.7 \ mm^2$ | $0.7 \ mm^{2}$ |

to the primary side to emulate the pack. The efficiency during the operation of the two modes is analyzed by a power analyzer (YOKOGAWAWT1804E).

For the power efficiency time trend test, the power efficiency is measured while the converter is operated for a 30-min bidirectional active balancing operation. The maximum initial voltage deviation between the cell voltages is set to 100mV for the balancing test. The time trend efficiency is also measured by a power analyzer. The temperature increase of the transformer is measured by a thermal camera (FLIR A70) after the 30-min operation.

4.2 Experimental results

The power efficiency test results are shown in Fig. 13. For the most of inductor current range, the proposed design achieves a higher efficiency in both operating modes, with about half the core volume when compared with the conventional design, which is shown in Table 6. This shows that the proposed design satisfies the required specifications with a higher efficiency and a reduced core volume than the conventional design.

Power efficiency time trend test results are shown in Fig. 14. The balancing algorithm toggles between the buck



Fig. 14 Converter power efficiency time trend test results

Table 7 Converter power efficiency time trend test results

| K_{gfe} | Proposed |
|-----------|---|
| 86.01 | 88.10 |
| 82.37 | 83.11 |
| 84.19 | 85.56 |
| | <i>K_{gfe}</i> 86.01 82.37 84.19 |



(a)



Fig. 15 Transformer temperature increase test: a conventional design; b proposed design

 Table 8
 Transformer temperature test results after 30 min

| Design | Temperature |
|------------------|-------------|
| Room temperature | 25 °C |
| Conventional | 34.16 °C |
| Proposed | 36.90 °C |



mode and boost mode every 20 s, which generates squarelike efficiency waveforms as shown Fig. 14. From the time trend test data, energy efficiency is calculated by integrating the power efficiency over the testing time and the results are summarized in Table 7. These results show that the proposed design achieves a 2% higher energy efficiency in the buck mode, a 0.7% higher energy efficiency in the boost mode, and a 1.5% higher overall energy efficiency than the conventional design method.

Finally, temperature increase test results of the transformer are shown in Fig. 15 and Table 8. The temperature increase of the proposed design sample is only 2.74 °C higher than that of the conventional design, which is mostly due to the reduced volume. However, this difference is trivial. In summary, the optimized transformer design achieves higher power and energy efficiency in the various ranges of the bidirectional converter operations with half of the core volume and a similar temperature increase.

5 Conclusion

A multiobjective transformer design optimization algorithm was proposed in this study. The proposed algorithm optimized the core volume and transformer loss at the same time. In the hardware verification, the proposed transformer design showed a 50% core volume reduction with higher power and energy efficiencies. Therefore, this algorithm was shown to be suitable for bidirectional applications that need a transformer with a compact volume.

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Data availability Data are available on request from the authorities.

References

- Tran, V.T., Islam, M.R., Muttaqi, K.M., Sutanto, D.: An efficient energy management approach for a solar-powered EV battery charging facility to support distribution grids. IEEE Trans. Ind. Appl. 55(6), 6517–6526 (2019)
- Boulanger, A.G., Chu, A.C., Maxx, S., Waltz, D.L.: Vehicle electrification: status and issues. Proc. IEEE 99(6), 1116–1138 (2011)
- 3. Sabillón Antúnez, C., Franco, J.F., Rider, M.J., Romero, R.: A new methodology for the optimal charging coordination of electric



vehicles considering vehicle-to-grid technology. IEEE Trans. Sustain Energy. **7**(2), 596–607 (2016)

- Fan, H., Li, H.: High-frequency transformer isolated bidirectional DC–DC converter modules with high efficiency over wide load range for 20 kVA solid-state transformer. IEEE Trans. Power Electron. 26(12), 3599–3608 (2011)
- Mohan, N., Undeland, T.M., Robbins, W.P.: Power Electronics: Converters, Applications, and Design, 3rd edn. John Wiley and Sons (2002)
- Erickson, R.W., Maksimovic, D.: Fundamentals of Power Electronics. Kluwer, Norwell (2001)
- Nijende, H., Frohleke, N., Bocker, J.: Optimized size design of integrated magnetic components using area product approach. 2005 European Conference on Power Electronics and Applications, Dresden, Germany, 10, (2005)
- Wu, H.H., Gilchrist, A., Sealy, K.D., Bronson, D.: A high efficiency 5 kW inductive charger for EVS using dual side control. IEEE Trans. Ind. Inf. 8(3), 585–595 (2012)
- Ta, L.A.D., Dao, N.D., Lee, D.-C.: High-efficiency hybrid LLC resonant converter for on-board chargers of plug-in electric vehicles. IEEE Trans. Power Electron. 35(8), 8324–8334 (2020)
- Zhao, B., Song, Q., Liu, W., Sun, Y.: A synthetic discrete design methodology of high-frequency isolated bidirectional DC/DC converter for grid-connected battery energy storage system using advanced components. IEEE Trans. Ind. Electron. 61(10), 5402– 5410 (2014)
- Kim, H.-S., Ryu, M.-H., Baek, J.-W., Jung, J.-H.: High-efficiency isolated bidirectional AC–DC converter for a DC distribution system. IEEE Trans. Power Electron. 28(4), 1642–1654 (2013)
- Wai, R.-J., Duan, R.-Y.: High-efficiency bidirectional converter for power sources with great voltage diversity. IEEE Trans. Power Electron. 22(5), 1986–1996 (2007)
- La, P.-H., Choi, S.-J.: Direct cell-to-cell equalizer for series battery string using switch-matrix single-capacitor equalizer and optimal pairing algorithm. IEEE Trans. Power Electron. 37(7), 8625–8639 (2022)
- Nguyen, N.A., La, P.H., Choi, S.J.: Coordinated operation algorithm of pack-chargers and cell-equalizers for SOC adjustment in second-life batteries. J. Power Electron 22, 105–115 (2022)
- 15. McLyman, C.W.T.: Transformer and Inductor Design Handbook, 4th edn. CRC Press (2011)
- De Nardo, A., Di Capua, G., Femia, N.: Transformer design for isolated switching converters based on geometric form factors of magnetic cores. IEEE Trans. Ind. Electron. 60(6), 2158–2166 (2013)
- Deb, K., Pratap, A., Agarwal, S., Meyarivan, T.: A fast and elitist multiobjective genetic algorithm: NSGA-II. IEEE Trans. Evol. Comput.Evol. Comput. 6(2), 182–197 (2002)
- Venkatachalam, K., Sullivan, C.R., Abdallah, T., Tacca, H.: Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters. Proc. IEEE Workshop Comput. Power Electron. 2, 36–41 (2002)
- Allmeling, J., Hammer, W., Schönberger, J.: Transient simulation of magnetic circuits using the permeance-capacitance analogy. 2012 IEEE 13th Workshop on Control and Modeling for Power Electronics (COMPEL), 1–6, (2012)
- Luo, M., Dujic, D., Allmeling, J.: Modeling frequency independent hysteresis effects of ferrite core materials using permeancecapacitance analogy for system-level circuit simulations. IEEE Trans. Power Electron. 33(12), 10055–10070 (2018)

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